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(54) Chip scale package

(57) A chip scale package structure suggested by the present invention for packaging an IC chip, is characterized by that: surrounding the IC chip by a package frame with a gap left between the IC chip and the package frame, extending at least two outer leads in opposite directions along the outer surface of the package frame, and connecting individually at least a pair of bonding points of the IC chip to the outer leads through a line (a bonding point through a line to a corresponding outer lead) comprising a connecting segment, the connecting segment being slant with upper end thereof connecting the outer lead and lower end thereof connected (may be through an inner lead) to the bonding point; the connecting segment is slant at an angle to the top outer surface of the package frame, thereby the gap and the angle can change with stress, whereby the chip scale package can cushion (buffer) a stress, particularly the stress resulting from a difference in coefficient of thermal expansion/shrinkage between the IC chip and the package frame. Another feature of the chip scale package structure is that the outer leads can be welded form three directions.

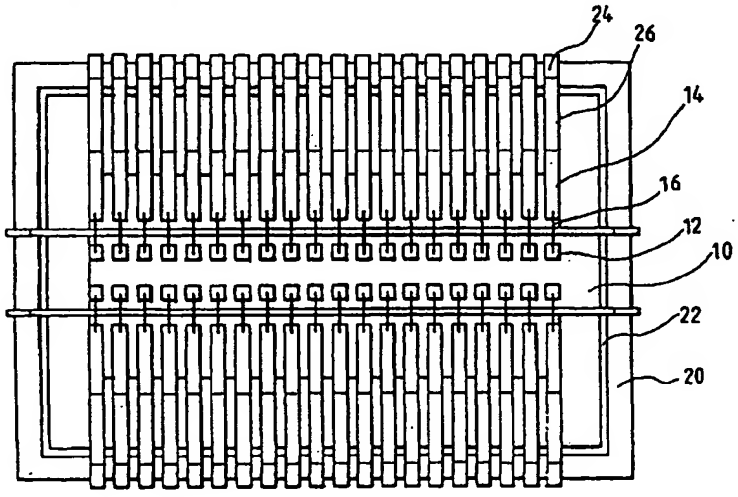

FIG. 1

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Description

FIELD OF THE INVENTION

[0001] The invention generally relates to an integrated circuit(IC) package, and particularly to a chip scale package of semiconductor device.

BACKGROUND OF THE INVENTION

[0002] Conventionally when packaging a semiconductor device, each bonding point of the IC chip to be packaged is connected with an inner lead through a bonding wire (such as a gold wire). Because each outer lead which is an extension of an inner lead can be welded into a connection point of a circuit board, a signal path can thus be built to conduct signal between a bonding point of the packaged IC chip and a corresponding connecting point of the circuit board. To prevent the bonding wire from being touched or hurt, encapsulant such as epoxy is used to cover the top of the IC chip. Due to possible existence of internal stress caused by the difference in coefficient of thermal expansion, a conventional IC package which usually lacks stress buffer capability tends to crack easily or to have its bonding wire broken away from its bonding point, resulting in bad application reliability of the IC. An IC chip without proper protection for either itself or its leads will likely be hurt or damaged by external force inherent in production process or shipping process, resulting in high failure rate of the IC. A conventional IC package with leads often deformed by external force or pressure needs work to recover the normal position of its leads, or to put its leads in order before welding them into another device such as a circuit board, leading to waste of labor and time in applying the IC. It can be seen now that there are disadvantages inherent in a conventional IC package structure, and there's a need of developing a new structure for overcoming these disadvantages.

SUMMARY OF THE INVENTION

[0003] The object of the present invention is to provide a new IC package structure with thin and super-mini size, and with features for overcoming the disadvantages inherent in a conventional IC package structure.

[0004] Another object of the present invention is to provide a new IC package structure allowing an IC package to be used for IC chip of various sizes, and therefore allowing lower production/storage cost.

[0005] A chip scale package structure based on the present invention for packaging an IC chip, is characterized by that:

surrounding the IC chip by a package frame with a gap left between the IC chip and the package frame, connecting (through a bonding wire and an inner lead, for example) at least a pair of bonding points of the IC chip individually to at least two outer leads both extending in opposite directions along the outer surface of the package frame, the package frame being prevented from moving beyond an assigned region by the outer leads, thereby the outer leads can be welded by approaching the top, side, and bottom outer surface of the package frame, whereby better adaptability of the chip scale package to various applications can be realized.

[0006] Another version of the chip scale package structure based on the present invention for packaging an IC chip, is characterized by that:

surrounding the IC chip by a package frame with a gap left between the IC chip and the package frame, extending at least two outer leads in opposite directions along the outer surface of the package frame, and connecting individually at least a pair of bonding points of the IC chip to the outer leads through a line (a bonding point through a line to a corresponding outer lead) comprising a connecting segment (and possibly a bonding wire as well as an inner lead), the connecting segment being slant with upper end thereof connecting the outer lead and lower end thereof connected to the bonding point; the connecting segment being slant at an angle to the connection point (right beside the top outer surface of the package frame) between the connecting segment and the outer lead, thereby the gap and the angle can change with stress, whereby the chip scale package can cushion (buffer) a stress, particularly the stress resulting from a difference in coefficient of thermal expansion/shrinkage between the IC chip and the package frame. It must be noted that the package frame's top surface beside which the connecting segment is connected with the outer lead is in a position above the bonding point, therefore the connecting segment is slant with an angle to the outer lead. Obviously the package frame can be prevented from moving beyond an assigned region as long as the outer leads extend throughout the outer surface of the package frame (including the part hooking upward under the IC chip).

A further version of the chip scale package structure based on the present invention for packaging an IC chip, is characterized by that:

surrounding the IC chip by a package frame with a gap left between the IC chip and the package frame, extending at least two outer leads in opposite directions along the outer surface of the package frame, and connecting individually at least a pair of bonding points of the IC chip to the outer leads through a bonding wire, an inner lead, and a connecting segment (a bonding point through a

bonding wire, an inner lead, and a connecting segment to an outer lead), the inner lead lying above the IC chip, the connecting-segment being slant with upper end thereof connecting the outer lead and lower end thereof connecting the inner lead. Obviously the chip scale package structure can be so configured that the package frame's top surface beside which the connecting segment is connected with the outer lead is in a position above the inner leads, therefore the connecting segment is slant with an angle to the outer lead.

A chip scale package for packaging an IC chip may be configured to comprise:

a package frame surrounding the IC chip with a gap between the package frame and the IC chip; and at least two outer leads connected to bonding points of the IC chip, extended in opposite directions along the outer surface of the package frame, and preventing the package frame from moving beyond an assigned region.

A chip scale package based on the present invention for packaging an IC chip, may also be configured to comprise: a package frame surrounding the IC chip with a gap between the package frame and the IC chip; at least two outer leads extending in opposite directions along the outer surface of the package frame; and a connecting segment being slant with upper end thereof connecting the outer lead and lower end thereof connected to a bonding point of the IC chip. Here the connecting segment may be connected to the bonding point through an inner lead which is above the top surface of the IC chip while in a position lower than the top outer surface of the package frame. Here the connecting segment may also be connected to the bonding point through an inner lead and a bonding wire, the inner lead is above the top surface of the IC chip while in a position lower than the top outer surface of the package frame.
The package frame may be made of material with high electrical conductivity, and may have its surface processed for electrical insulation , thereby the induction of the outer lead can be lowered.
The package frame may also be made of material with high heat dissipation capability, thereby the heat generated by the IC chip can be easily dissipated. The outer lead's end which is under the IC chip may be configured to hook against the package frame to prevent the package frame from moving beyond an assigned region. It may also be configured to just hook upward to prevent the package frame from moving beyond an assigned region.
It can be seen the slant angle of the connecting segment can change with a stress, thereby the chip scale package can cushion a stress.

[0007] The chip scale package according to the present invention may also be configured to further comprise material covering the top surface of the IC chip, thereby the bonding wire and the bonding points can be protected.

[0008] It must be noted the chip scale package based on the present invention may be so configured that the magnitudes of the gap and the angle are in such a range that a stress caused by a difference in coefficient of thermal expansion/shrinkage between the IC chip and the package frame can be perfectly cushioned.

[0009] The present invention may best be understood through the following description with reference to the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0010]

Fig. 1 is a top view of an embodiment based on the present invention.
Fig. 2 is a bottom view of a embodiment based on the present invention.
Fig. 3 is a side view of an embodiment based on the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0011] A preferred embodiment of the chip scale package based on the invention is illustrated by Fig. 1, Fig. 2, and Fig. 3. As shown in these figures, the bonding points 12 on the top of IC chip 10 are connected with inner lead 14 through bonding wires 16 (such as gold wires). Material such as epoxy is used to cover the top of IC chip 10 for preventing bonding 16 wires from being damaged in production processing or product application phase. IC chip 10 is surrounded by a package frame 20 with a gap 22 between them (between IC chip 10 and package frame 20). Package frame 20 is made of material with high electrical conductivity and heat dissipation capability, and has its surface processed for insulation capability, resulting in good heat dissipating for an operating IC chip, and lower induction for outer lead 24, and consequently higher operating reliability and better quality of signal communication can be achieved. Inner lead 14 and outer lead 24, connected by a connecting segment 26, can be deemed an element in spite of different names assigned for the reason they are differently located. Connecting segment 26 is configured to slant, with upper end connected with outer lead 24 and lower end connected with inner lead 14. Outer lead 24 extends along the outer surface of package frame 20 (of course bends according to the shape of package frame 20), and ends under IC chip 10 to hook upward for fixing package frame 20 (to hook the end of the part of package frame 20 which is under IC chip 10, for example), or for limiting package frame 20 to an optimum working position (or region). With outer lead 24 extending along the top, side, and bottom face of

package frame 20, A (top segment of outer lead 24), B (side segment of outer lead 24), and C (bottom segment of outer lead 24) are available for welding, thereby an IC package so configured can adapt to various applications in which different portions of an IC package is to be selected for welding operation.

[0012] As long as package frame 20 is made to be of high mechanical strength (capable of withstanding pressure or stress, for example) and with surface flat enough, IC chip 10 can be protected from damage possibly caused in each production phase as well as shipping phase. Supported by package frame 20, outer lead 24 can resist high pressure in molding, testing, and welding processes. Pressure may be exerted on A (top segment of outer lead 24), B

(side segment of outer lead 24), and C (bottom segment of outer lead 24) of outer lead 24 to make them stick evenly to the surface of package frame 20, thereby to realize a perfect contact between outer lead 24 and the face of an object whenever necessary. Obviously either A (top segment of outer lead 24), or B(side segment of outer lead 24), or C (bottom segment of outer lead 24) of all outer leads 24 can be easily adjusted to be on the same plane (all outer leads 24 with A on the same plane, with B on another plane, foe example), to achieve optimum contacting between outer lead 24 and the object to be welded. It is clear the chip scale package structure based on the present invention can solve a troublesome problem that a conventional IC package hardly has its all package leads lying on the sane plane. The pressure exerted on A (top segment of outer lead 24), B (side segment of outer lead 24), and C (bottom segment of outer lead 24) of outer lead 24 can be prevented form reaching IC chip 10 according to the structure (gap 22 contributes to this effect, for example). It can be seen now the chip scale package structure based on the invention provides an IC package with high reliability, pressure resistance, and significant convenience of welding operation for various applications. The gap 22 between IC chip 10 and package frame 20, together with the connecting segment 26 which slants with an angle and connects with inner lead 14 and outer lead 24, function as a stress buffer mechanism, because the position (height, for example) of IC chip 10 can adapt to the effect of thermal expansion/ shrinkage through changing the slant angle of connecting segment 26, thereby the stress caused by the effect of thermal expansion/ shrinkage can be buffered (lowered), whereby an IC package of such a structure can be applied wherever high reliability is required.

[0013] The fact that the structure based on the invention can provide an IC package with resistance to thermal expansion stress resulting from thermal coefficient difference is further described as follows.

[0014] Suppose the thermal coefficient of package frame 20 is bigger than IC chip 10 , and IC chip 10 generates heat when operating, package frame 20 will expand outward more than IC chip 10 then (magnitude of expansion size of package frame 20 is bigger than that of IC chip 10), resulting in smaller slant angle of connecting segment 26 connecting inner lead 14 and outer lead 24, consequently leading to moving of IC chip 10 upward, and buffer (or cushioning) for stress; when IC chip 10 cools as a result of being idle (not operating), package frame 20 shrinks inward more than IC chip 10 then (magnitude of shrinkage of package frame 20 is bigger than that of IC chip 10), leading to bigger slant angle of connecting segment 26, consequently IC chip 10 moves downward and buffer (or cushioning) for stress is provided.

[0015] On the contrary, in case the thermal coefficient of package frame 20 is smaller than IC chip 10 , and IC chip 10 generates heat when operating, IC chip 10 will expand outward more than package frame 20 then (magnitude of expansion size of IC chip 10 is bigger than that of package frame 20), resulting in bigger slant angle of connecting segment 26 connecting inner lead 14 and outer lead 24, consequently leading to moving of IC chip 10 downward, and buffer (or cushioning) for stress; when IC chip 10 cools as a result of being idle (not operating), IC chip 10 shrinks inward more than package frame 20 then (magnitude of shrinkage of IC chip 10 is bigger than that of package frame 20), leading to smaller slant angle of connecting segment 26, consequently IC chip 10 moves upward and buffer (or cushioning) for stress is provided.

[0016] It is clear now that the IC package structure based on the invention and illustrated above can realize the following advantages over conventional arts:

1. package frame 20 of fixed size can be used for IC chip 10 of various sizes, resulting in IC package of just one size, leading to lower cost for fixture as well as production and application.
2. package frame 20 of accurate size enables easy positioning of automatic machinery for assembly process.
3. package frame 20 with surface processed for insulation can effectively lower the induction of outer lead 24.
4. package frame 20 of high thermal conductivity can effectively dissipate the power generated by IC chip 10, leading to high reliability of IC chip 10.

In conclusion, the IC package structure based on the invention has never been found up to now. It can realize some significant practical efficacy as well as better performance progress/application flexibility/environmental adaptability compared with conventional arts.

[0017] While the invention has been described in terms of what are presently considered to be the most practical and preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims

which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.

Claims

1. A chip scale package structure to be applied to packaging an IC chip, is characterized by that:

   said IC chip being surrounded by a package frame with a gap between said IC chip and said package frame, bonding points of said IC chip being connected to at least two outer leads both extending in opposite directions along the outer surface of said package frame, and preventing said package frame from moving beyond an assigned region

2. A chip scale package structure to be applied to packaging an IC chip, is characterized by that:

   said IC chip being surrounded by a package frame with a gap between said IC chip and said package frame, at least two outer leads being extended in opposite directions along the outer surface of said package frame, and connected individually to at least two bonding points of said IC chip through a connecting segment which is slant with upper end thereof connecting said outer lead and lower end thereof connected to said bonding point.

3. A chip scale package structure to be applied to packaging an IC chip, is characterized by that:

   said IC chip being surrounded by a package frame with a gap between said IC chip and said package frame, at least two outer leads being extended in opposite directions along the outer surface of said package frame, and connected individually to at least two bonding points of said IC chip through a bonding wire, an inner lead, and a connecting segment, said inner lead lying above said IC chip, said connecting segment being slant with upper end thereof connecting said outer lead and lower end thereof connecting said inner lead.

4. A chip scale package for packaging an IC chip, comprising:

   a package frame surrounding said IC chip with a gap between said package frame and said IC chip;
   at least two outer leads connected to bonding points of said IC chip, extended in opposite directions along the outer surface of said package frame, and preventing said package frame from moving beyond an assigned region.

5. A chip scale package for packaging an IC chip, comprising:

   a package frame surrounding ,said IC chip with a gap between said package frame and said IC chip;
   at least two outer leads extending in opposite directions along the outer surface of said package frame; and
   a connecting segment being slant with upper end thereof connecting said outer lead and lower end thereof connected to a bonding point of said IC chip, thereby said outer leads can be welded from the top, side, and bottom outer surface of said package frame, and both said gap and the slant angle of said connecting segment can change in response to a stress, whereby a stress can be cushioned.

6. The chip scale package according to claim 5 wherein said connecting segment is connected to said bonding point through an inner lead which is above the top surface of said IC chip while in a position lower than the top outer surface of said package frame.

7. The chip scale package according to claim 5 wherein said connecting segment is connected to said bonding point through an inner lead and a bonding wire, said inner lead is above the top surface of said IC chip while in a position lower than the top outer surface of said package frame.

8. The chip scale package according to claim 5 wherein said package frame is made of material with high electrical conductivity, and has surface thereof processed for electrical insulation, thereby the induction of said outer lead can be lowered.

9. The chip scale package according to claim 5 wherein said package frame is made of material with high heat dissipation capability, thereby the heat generated by said IC chip can be easily dissipated.

10. The chip scale package according to claim 5 wherein said outer lead's end which is under said IC chip hooks against said package frame to prevent said package frame from moving beyond an assigned region.

11. The chip scale package according to claim 5 wherein said outer lead's end which is under said IC chip hooks upward to prevent said package frame from moving beyond an assigned region.

12. The chip scale package according to claim 5 wherein said connecting segment is slant at an angle which changes with a stress, thereby said chip scale package can cushion a stress.

13. The chip scale package according to claim 6 wherein said connecting segment is slant at an angle to the top outer surface of said package frame, said angle changes with a stress, thereby cushions a stress.

14. The chip scale package according to claim 7 further comprising material covering the top surface of said Ic chip, thereby said bonding wire and said bonding points can be protected.

15. The chip scale package according to claim 13 wherein the magnitudes of said gap and said angle are in such a range that a stress caused by a difference in coefficient of thermal expansion between said IC chip and said package frame can be cushioned.

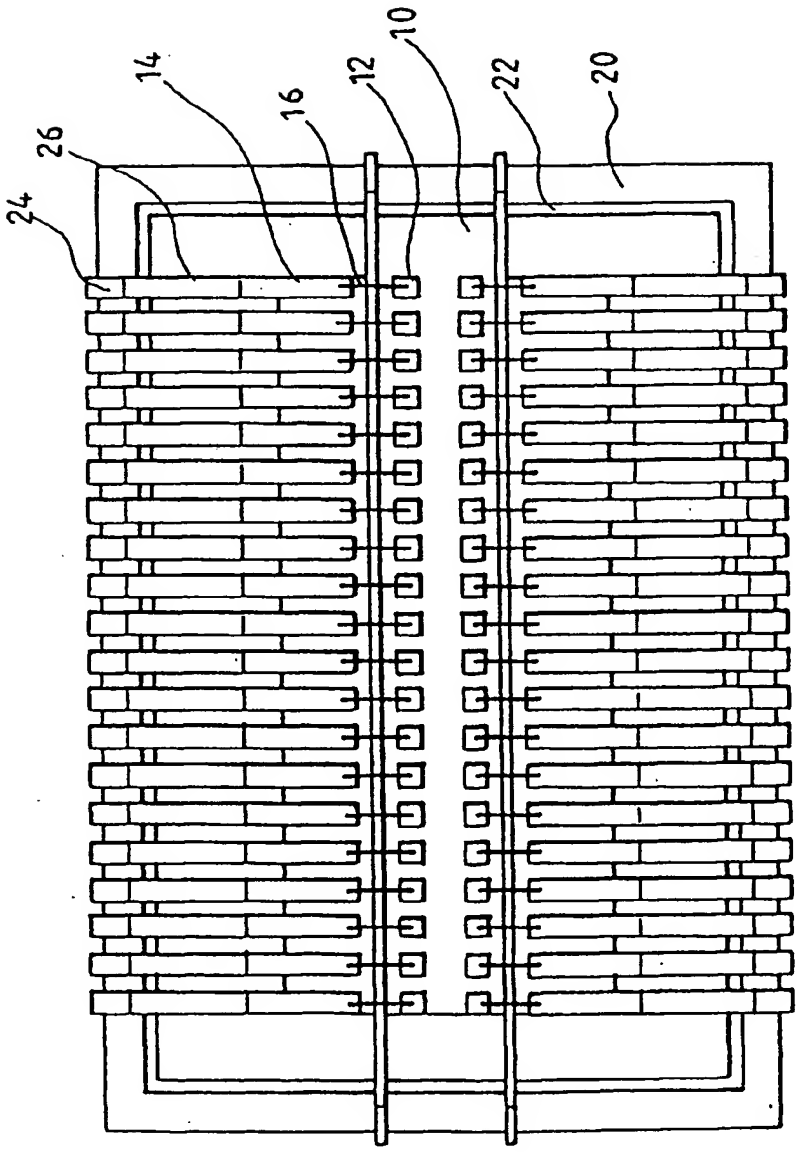

FIG. 1

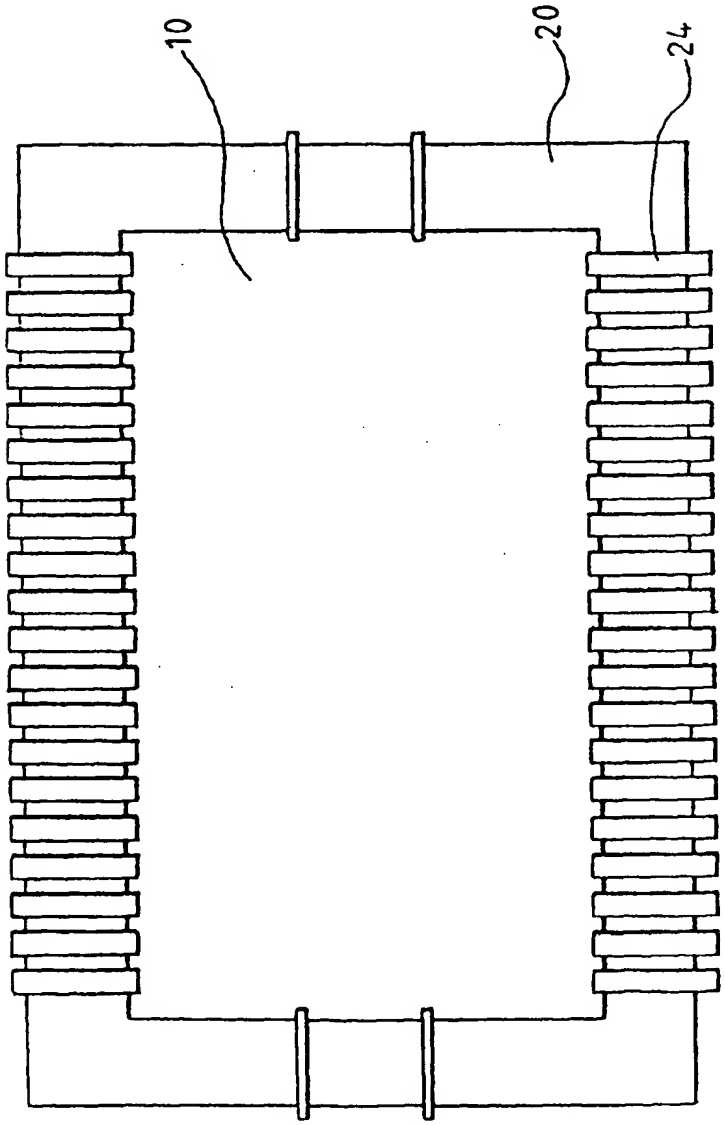

FIG.2

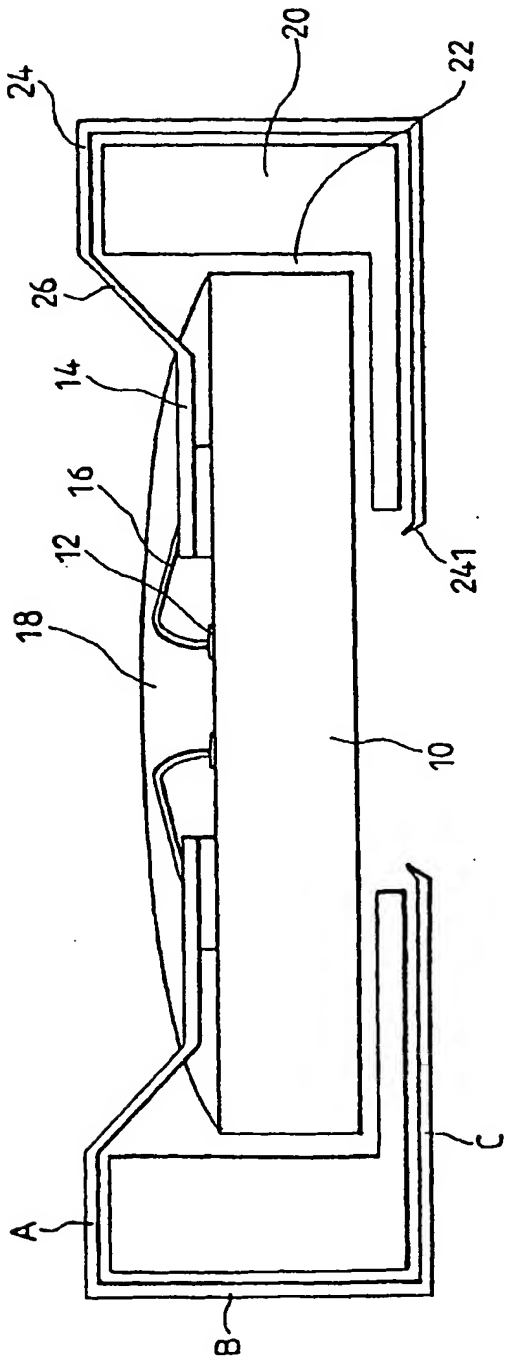

FIG.3

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EUROPEAN SEARCH REPORT

Application Number
EP 98 30 2098

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	US 5 347 159 A (KHANDROS IGOR Y ET AL) 13 September 1994 * column 7, line 51 - column 8, line 7; figures 4,5,7 *	1,4 2,3,5,8, 9,14	H01L23/495
A	PATENT ABSTRACTS OF JAPAN vol. 096, no. 012, 26 December 1996 -& JP 08 213424 A (FUJITSU LTD), 20 August 1996 * abstract; figures 2A,2B,3A,3B *	1-5	
A	PATENT ABSTRACTS OF JAPAN vol. 096, no. 001, 31 January 1996 -& JP 07 249725 A (FURUKAWA ELECTRIC CO LTD:THE), 26 September 1995 * the whole document *	1-5	
Y	US 5 362 656 A (MCMAHON JOHN F) 8 November 1994 * the whole document *	2,3,5,8, 9,14	
A	PATENT ABSTRACTS OF JAPAN vol. 097, no. 008, 29 August 1997 -& JP 09 092769 A (HITACHI CABLE LTD), 4 April 1997 * abstract; figures 1,3,4 *	1-5	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	PATENT ABSTRACTS OF JAPAN vol. 096, no. 005, 31 May 1996 -& JP 08 017864 A (NEW JAPAN RADIO CO LTD), 19 January 1996 * abstract *	1-5	
A	PATENT ABSTRACTS OF JAPAN vol. 095, no. 006, 31 July 1995 -& JP 07 078925 A (MATSUSHITA ELECTRIC IND CO LTD), 20 March 1995 * the whole document *	1-5	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 August 1998	Zeisler, P

CATEGORY OF CITED DOCUMENTS

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